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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/534,143	06/21/2006	Hiroyuki Nagasaka	12000.SMG.0052	4832

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North Star Intellectual Property Law, PC
P.O. Box 34688
Washington DC, DC 20043

EXAMINER	
GARCIA, SANTIAGO	

ART UNIT	PAPER NUMBER
2611	

MAIL DATE	DELIVERY MODE
11/24/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/534,143	NAGASAKA, HIROYUKI	
	Examiner	Art Unit	
	SANTIAGO GARCIA	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 July 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 7-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 7-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 July 2009* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see page 11, filed 7/08/09, with respect to **all** objections to the drawings have been fully considered and are persuasive. The objections of the first office action dated 05/13/09 has been withdrawn due to applicant's amendment that does not include new matter.

2. Applicant's arguments, see page 11, filed 7/08/09, with respect to the double patenting rejection have been fully considered and ***are NOT*** are persuasive. Although the terminal disclaimer has been filled, it was denied by the office due to lack of payment. The fee must be paid in order to over come the double patenting rejection. Therefore the double patenting rejection stands.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting

ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

1. Claims 1-4 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-2, 4-5, 7 and 8 of U.S. Patent No. 7,359,425 to Yoshio Wada in view of patent number 5,533,010 to Tanaka and in view of Shimokoriyama US 5,617,143. Although the conflicting claims are not identical, they are not patentably distinct from each.

Application Claim 1, and US patent claim 1 are both drawn to the same invention, i.e. an ultra wideband radio transmitter. These claims differ in scope in that application claim 1 with additional limitations, i.e., a local oscillator for outputting a local signal for frequency-converting a corresponding addition signal at a high frequency band or a low frequency band; a mixer for receiving the addition signal and the local signal, and frequency-converting the corresponding addition signal; and an antenna for receiving the frequency-converted addition signal and radiating the corresponding signal in the air, is narrower in scope than US patent claim 1.

Tanaka discloses a local oscillator for outputting a local signal for frequency-converting a corresponding addition signal at a high frequency band or a low frequency band (Tanaka, (6) "and at 135 a local oscillator for outputting a signal to the mixer circuit above or other components"); a mixer for receiving the addition signal and the local signal (Tanaka, fig.3 Mixer 133.), and frequency-converting the corresponding addition signal (Tanakafig.3 shows a connection from local oscillator 135 to mixer 133); and an antenna for receiving the frequency-

converted addition signal and radiating the corresponding signal in the air (Tanaka, fig.3 antenna 100.).

Therefore it would have been obvious to one of ordinary skill in the art at the time to which the invention was made to modify US patent claim 1 with the teaching of Tanaka by integrating a local oscillator with a mixer.

The motivation would be to have an up converter (mixer and local oscillator) to be able to transmit the data to the receiver as the prescribed frequency band as configurable.

Allowance of application claim 1 would result in an unjustified time-wise extension of the monopoly granted for the invention defined by US patent claim 1. Therefore, obviousness-type double patenting is appropriate.

Application claim 2 corresponds to US patent claim 2.

Application Claim 3, and US patent claim 4 are both drawn to the same invention, i.e. an ultra wideband radio receiver. These claims differ in scope in that application claim 3 with additional limitations, i.e., a local oscillator for outputting a local signal for frequency-converting the radio wave signal; a mixer for receiving the radio wave signal and the local signal, and frequency-converting the radio wave signal;, is narrower in scope than US patent claim 4.

Tanaka discloses a local oscillator for outputting a local signal for frequency-converting the radio wave signal (Tanaka, (6) "and at 135 a local oscillator for outputting a signal to the mixer circuit above or other components") ; a mixer for receiving the radio wave signal and the local signal, and frequency-converting the radio wave signal (Tanaka, fig.3 Mixer 153).

Therefore it would have been obvious to one of ordinary skill in the art at the time to which the invention was made to modify US patent claim 4 with the teaching of Tanaka by integrating a local oscillator with a mixer.

The motivation would be to have a down converter (mixer and local oscillator) to be able to receive the data from the receiver as the prescribed frequency band as configurable.

Yoshio in view of Tanaka does not clearly teach, wherein the delay time measurer comprises a first circuit for receiving the first output signal and calculating a square value or an absolute value of the first output signal, a second circuit for receiving the second output signal and calculating a square value or an absolute value of the second output signal, a first latch for receiving and setting a output signal of the first circuit, a second latch for receiving and setting a output signal of the second circuit, a first memory for reading a output signal of the second latch as the detection result by receiving a output signal of the first latch, a second memory for reading the output signal of the first latch as the detection result by receiving the output signal of the second latch, and a reset section for outputting a reset signal by receiving outputs of the first and second latches.

Shimokoriyama teaches, wherein the delay time measurer comprises a first circuit for receiving the first output signal and calculating a square value or an absolute value of the first output signal (Shimokoriyama, fig.4 204 absolute value circuit),

a second circuit for receiving the second output signal and calculating a square value or an absolute value of the second output signal (Shimokoriyama, fig.4 213 second absolute value circuit),

a first latch for receiving and setting a output signal of the first circuit (Shimokoriyama, fig.4 213 second absolute value circuit then going to D-latch 207),

a second latch for receiving and setting a output signal of the second circuit (Shimokoriyama, fig.4 213 second absolute value circuit then going to D-latch 216),

a first memory for reading a output signal of the second latch as the detection result by receiving a output signal of the first latch (Shimokoriyama, fig.4 element 208 receiving the output of 207 which decides the output and reads out the output signal 210, see col 5 lines 55-62) ,

a reset section for outputting a reset signal by receiving outputs of the first and second latches (Shimokoriyama, fig.4 control unit 209 controlling 206 and 215 which going down to "0" will be resetting the latches 207 and 216).

At the time at which the invention was made it would have been obvious to one of ordinary skill in the art to include the circuit of Shimokoriyama in fig.4 inside of the delay time measurer of Yoshio.

The motivation would have been to have a more reliable system by delaying multiple parts of the signal to create a better channel.

Applicant Admitted Prior Art in view of Tanaka and further in view of Shimokoriyama US 5,617,143 teach all the limitations as applied above.

Except for a second memory for reading the output signal of the first latch as the detection result by receiving the output signal of the second latch.

Examiner takes official notice here since it is well known in the art to have a second memory for reading the output signal of the first latch as the detection result by receiving the output signal of the second latch.

It would have been obvious to one of ordinary skill in the art at the time at which in the invention was made to add a duplicate circuit of the second and second memory to read out the results of the latches since three signals are going out.

The motivation would to improve system reliability and to reduce system interference.

Allowance of application claim 3 would result in an unjustified time-wise extension of the monopoly granted for the invention defined by US patent claim 4. Therefore, obviousness-type double patenting is appropriate.

Application claims 4, 5 and 6 correspond to US patent claim 5, 7 and 8 respectively.

Conclusion

2. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SANTIAGO GARCIA whose telephone number is (571)270-5182. The examiner can normally be reached on MONDAY- FRIDAY 7:30 AM - 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hai, Tran can be reached on (571) 272-3011. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/SG/
/CHIEH M FAN/

Supervisory Patent Examiner, Art Unit 2611